

Multilayer Ceramic Chip Capacitor

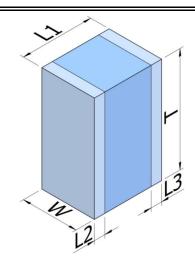
Part Number: 1210J6300473JCTVM2

Description: 1210 630Vdc 47nF ±5% C0G/NP0 (1B)

A range of C0G/NP0 MLC capacitors to suit a variety of applications. Available in a wide selection of chip sizes, working voltages and termination options, including FlexiCap™, the world's first commercially available flexible termination.

Suffix code PXX or PX mandates the use of precious metal electrode (PME) materials. This may incur additional costs.

Parts suffix coded VM2 are designed and qualified for mounting as 1210 case size with increased thickness. Please refer to the factory to discuss mounting in alternative ways.



Mechanical Specification

Size Code

Length (L1) in mm (")

Width (W) in mm (")

Thickness (T) in mm (")

Minimum Termination Band (L2,L3) in mm (") Maximum Termination Band (L2,L3) in mm (")

Termination Material

Solderability Packaging

Conformal Coating

1210

3.2 +0.50/-0.20 (0.126 +0.020/-0.008)

2.5 +0.40/-0.20 (0.098 +0.016/-0.008)

6.0±0.25 (0.236±.010)

0.25 (0.010)

0.75 (0.030)

Nickel Barrier, Sn Plated Solder (RoHS compliant)

IEC-60068-2-58

7" Reel Horizontal Orientation, 300 per reel

Not normally required

General Electrical Specification

Rated Voltage

Nominal Capacitance Value

Capacitance Tolerance

Tangent of Loss Angle (Tan δ)

Capacitance and Tan δ Test Conditions

Voltage Proof

(Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH)

Min Insulation Resistance (IR)

Dielectric Classification

Rated Temperature Range

Maximum Capacitance Change over Temperature Range

Climatic Category (IEC) Ageing Characteristic

630Vdc

47nF

±5%

≤0.001

1.0Vrms @ 1kHz

945Vdc

21.28GOhm @ 100Vdc

C0G/NP0 (1B)

-55°C / +125°C

No DC Voltage 0±30ppm/°C

Rated DC Voltage -

55/125/56

Zero

Knowles Precision Devices - Sales

Europe: KPD-Europe-sales@knowles.com

Asia: KPD-Asia-sales@knowles.com

USA: KPD-NA-sales@knowles.com

www.knowlescapacitors.com

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Data is correct to the best of our knowledge, errors and

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Date: Wednesday, September 03, 2025



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Part Number: 1210J6300473JCTVM2

Description: 1210 630Vdc 47nF ±5% C0G/NP0 (1B)

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU

Compliant

REACH Compliant

250 compliant

California Proposition 65

No exposure risk

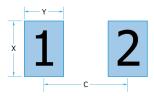
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

IPC-7351 pad design

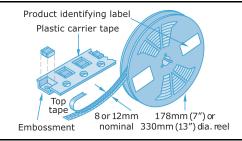
	1210	
С	3.00mm	0.118"
Υ	1.15mm	0.045"
X	2.70mm	0.106"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Soldering

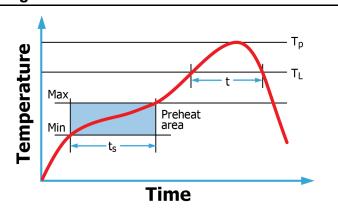
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

DLI



Application notes with mounting and handling guidance are available on request.

Knowles Precision Devices - Sales

Europe: KPD-Europe-sales@knowles.com

Compex

Asia: KPD-Asia-sales@knowles.com

USA: KPD-NA-sales@knowles.com

www.knowlescapacitors.com

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